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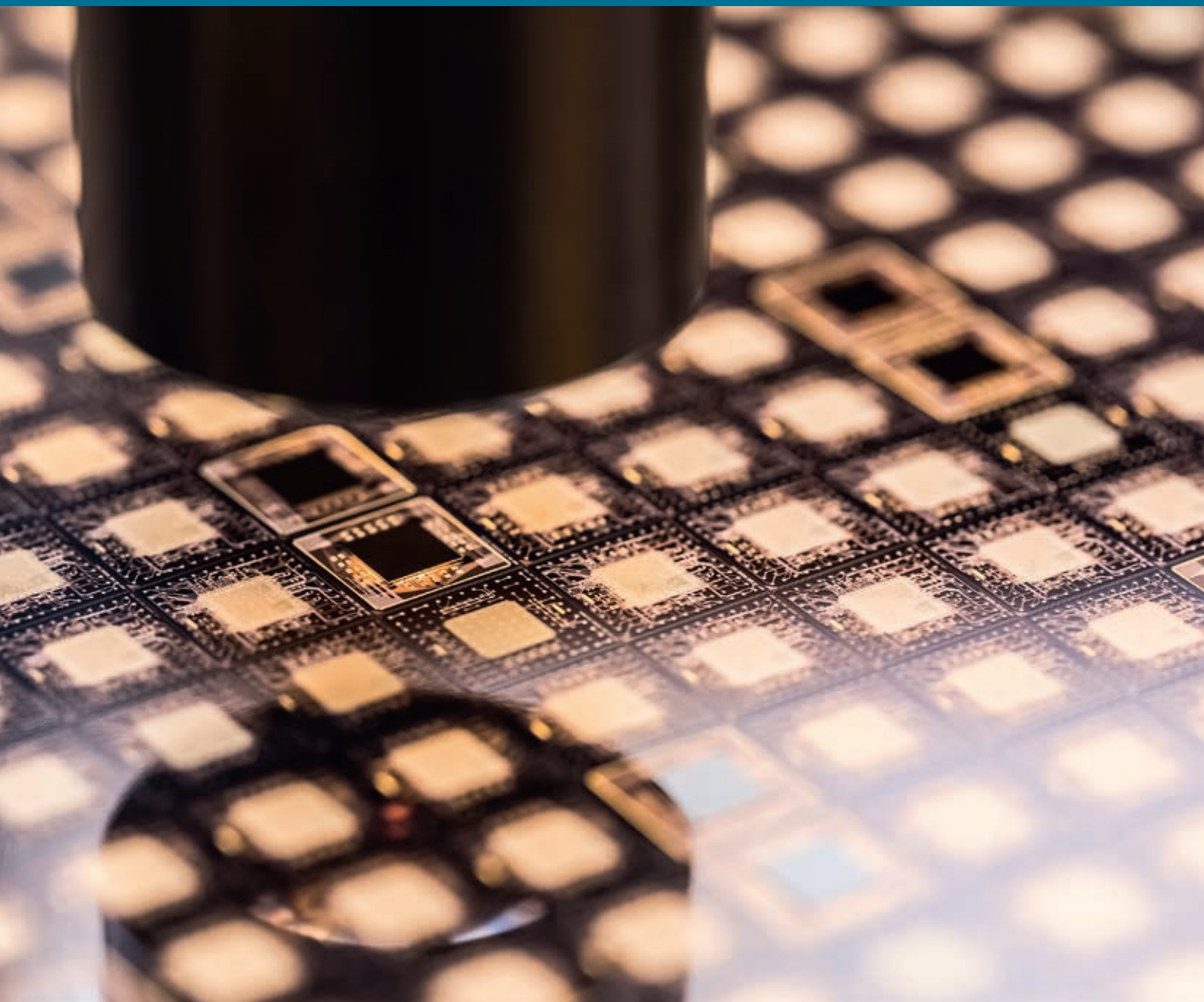
FRAUNHOFER INSTITUTE FOR RELIABILITY AND MICROINTEGRATION IZM

DEPARTMENT
WAFER LEVEL SYSTEM INTEGRATION
ALL SILICON SYSTEM INTEGRATION DRESDEN – ASSID



ALL SILICON SYSTEM INTEGRATION DRESDEN FRAUNHOFER IZM-ASSID

FRAUNHOFER IZM

The Fraunhofer Institute for Reliability and Microintegration IZM is one of 72 Fraunhofer institutes conducting contract research for customers from industry and the public sector in Germany. The Fraunhofer-Gesellschaft is the leading organization for applied research in Europe. Fraunhofer IZM is a worldwide renowned institute specialized in the development of advanced packaging and system integration technologies, which are then transferred to industry. The institute is thus able to offer customer-specific solutions for microelectronic products in the overall scope of smart system integration.

FRAUNHOFER IZM-ASSID

Fraunhofer IZM's center "All Silicon System Integration Dresden – ASSID" operates a leading-edge, industry-compatible 200/300 mm 3D wafer-level process line (ISO 9001-15) with modules for TSV formation, pre-assembly (thinning, singulation), wafer-level assembly and stack formation. ASSID focuses on process development, material and equipment evaluation as well as R&D services and prototyping for small to mid-size volume manufacturing. It is a partner in national, European and worldwide industrial and scientific projects and networks for 3D system integration, e. g. HIR, HTA, ENIAC JU, Catrene, H 2020, SEMATECH and the Silicon Saxony Network. Fraunhofer IZM-ASSID has established cooperation and joint development programs with industrial partners for undertaking material and equipment evaluation, process development as well as process product integration. Fraunhofer IZM is a member of the "Research Fab Microelectronics Germany"

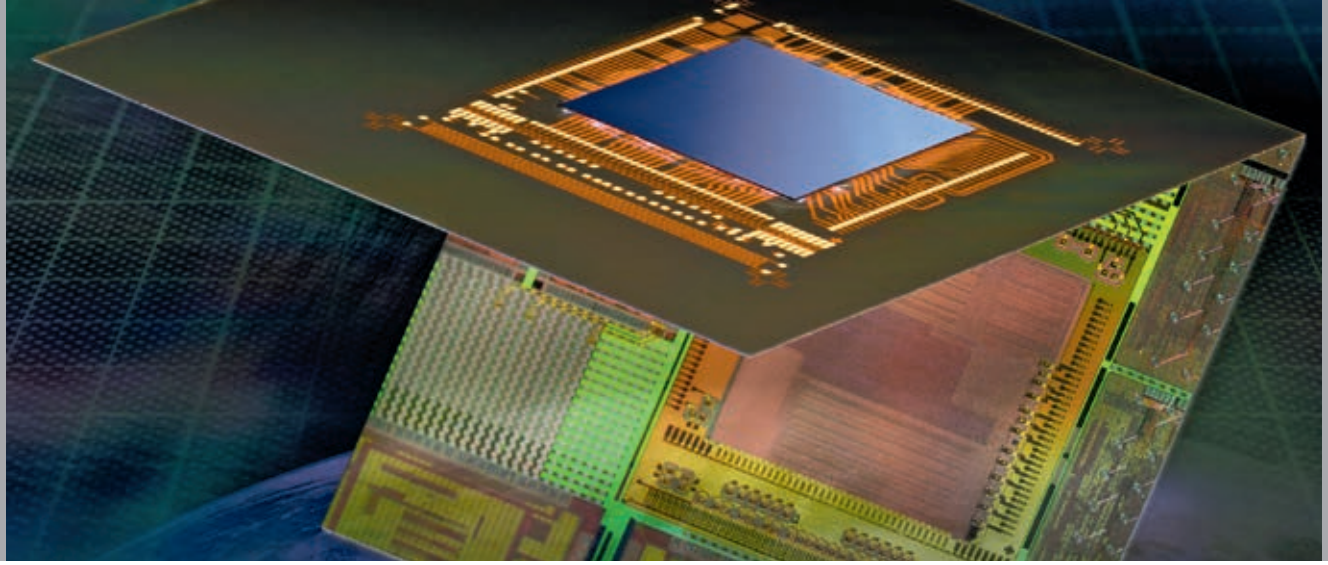
COOPERATION ACTIVITIES

Within the realms of academia, IZM-ASSID is cooperating with

- Technische Universität Dresden (Electronic Packaging Laboratory, IAVT)
- Technische Universität Berlin
- Technische Universität Chemnitz
- International research labs in Europe, USA and Asia

Fraunhofer IZM-ASSID has established close collaborations especially with the Saxony-based Fraunhofer institutes. Besides joint projects and services, these activities include:

- Fraunhofer Cluster 3D Integration:
  To address the technological complexity of 3D integration, leading Fraunhofer institutes cluster their outstanding competencies in the fields of technology, design, analytics and reliability to cover a broad spectrum of topics.
  www.3D-integration.fraunhofer.de
- High Performance Center Functional Integration in Micro- and Nanoelectronics:
  Fraunhofer IZM, IIS-EAS, IPMS, ENAS, TU Dresden and TU Chemnitz cluster their competencies in the fields of micro/nano electronics and thus strengthen the competitive and innovative capacity of the Free State of Saxony. Research know-how will – in close cooperation with resident companies – be extended and innovations can be implemented more quickly into applications and products.
- Research Fab Microelectronics Germany
  https://www.forschungsfabrik-mikroelektronik.de/



HETEROGENEOUS 3D WAFER-LEVEL SYSTEM INTEGRATION

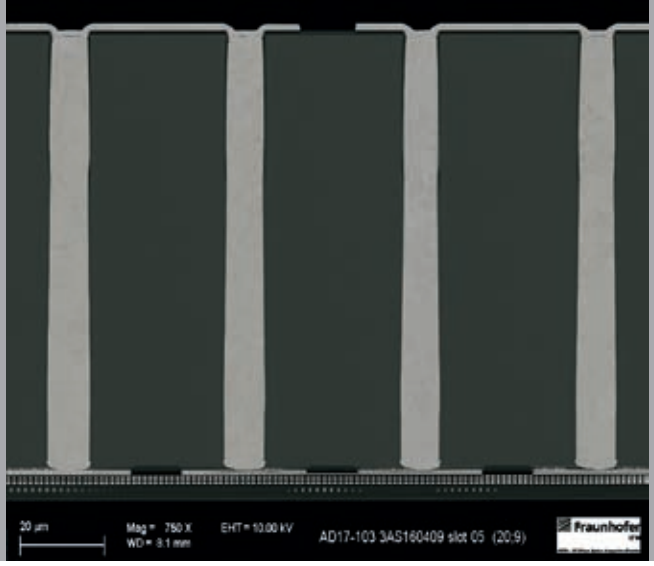
3D integration is of high significance for the realization of future innovative products and a key enabler to meet technical requirements e.g. performance, form factor and functionality for smart systems in application fields like information and communication, security, healthcare, mobility and transportation and industrial electronics. It allows the multi-device integration of analog and digital devices e.g. sensors, MPU, ASICs and transceivers into one optimized wafer-level system-in-package (WL-SiP). Therefore, scientific and industrial research is focusing on developing 3D heterogeneous integration technologies to enable 3D smart systems.

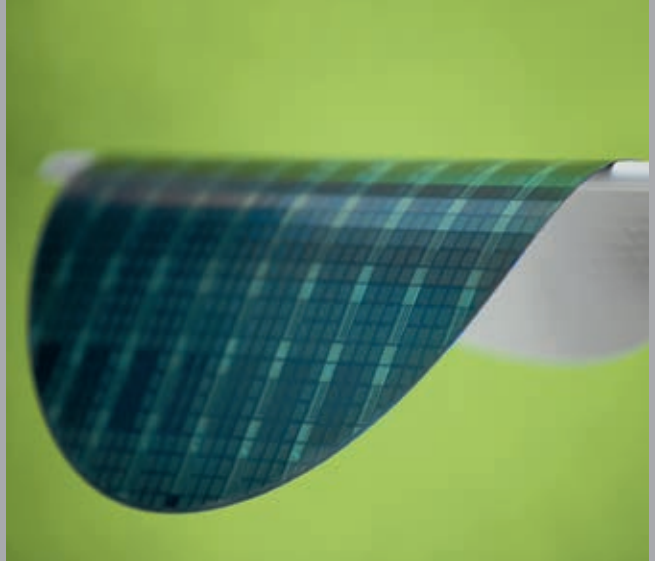
3D Wafer-level System in Package

Fraunhofer IZM-ASSID provides prototyping and low-volume manufacturing services (300/200 mm) at its advanced pilot line for wafer-level packaging. Fraunhofer IZM-ASSID has established strong cooperation with leading material and equipment suppliers in which customer-specific solutions in the fields of material, equipment and processes are developed and introduced into products. As a member of the Fraunhofer Cluster 3D Integration and Research Fab Microelectronics Germany, Fraunhofer IZM-ASSID offers – together with its Fraunhofer partners – fully customized support for 3D integration including design, technology and reliability. The pilot line is certificated according ISO 9001-15.

Core Competencies:

- Leading-edge micro-electronic packaging
- 3D heterogeneous system integration
- Wafer-level system-in-packages (WL-SiP)
- Enhanced interconnection and assembly technologies
- Customized process and technology development
- Customer-specific prototyping and pilot-line manufacturing
- Process, equipment and material evaluations as well as qualification
- Process transfer and product integration





COPPER THROUGH SILICON VIA (TSV) FORMATION

Through silicon vias (TSVs) are a key element in 3D wafer-level system integration. Fraunhofer IZM-ASSID has developed a TSV process (POR) for customer-defined applications based on Cu-ECD.

All processes are carried out using advanced, industry-compatible process equipment for 200/300 mm wafers.

Research and development focus:

- High-density Cu-TSV technology (via-last, via-middle, backside via-last) for active circuit devices and interposers
- Application-specific TSV dimensions diameter/depth:
  … min. 5 µm/80 µm
  … typ. 10 µm/150 µm
  … backside TSV (Cu-liner) up to 250–700 µm depth
- Cu-TSV filling using high-speed ECD
- Evaluation and qualification of new materials for isolation, barrier/seed and TSV filling
- Optimized via reveal

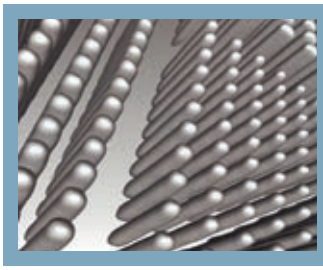
WAFER THINNING AND THIN WAFER HANDLING

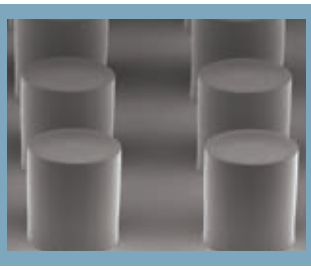
Wafer thinning and thin wafer handling technologies are an integral part of the TSV process integration and it is essential for all 3D stacked wafer or die architectures.

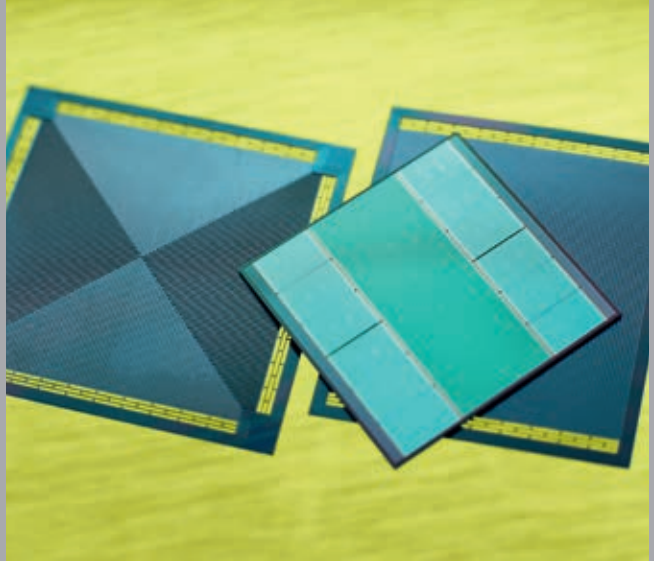
Continuous optimization of these technologies is indispensable to meet the requirements of cost-effective manufacturing and the realization of 3D systems.

Research and development focus:

- Optimization of temporary wafer-bonding and de-bonding technologies (device wafer thickness: > 20 µm; multiple repeatable bonding and de-bonding processes)
- Enhanced wafer thinning and stress relief technologies for ultra-thin wafers (> 20 µm, 12")
- Enhanced singulation technologies e.g. stealth dicing for low k-materials, small dicing streets (< 40 µm) and reduced mechanical edge and corner damage to wafer frontside and backside







INTERPOSERS WITH HIGH-DENSITY REDISTRIBUTION

The TSV interposer is used as a carrier to meet the technical specifications of integrated circuits e. g., geometry, high number of I/O and their high-density routing. The functionality of Si-interposers will be extended by the integration of passive devices such as inductors, resistors and capacitors – with an emphasis on RF applications. Latest generations also include multiple integrated active devices e. g. MPU, memories and sensors and deal with high power dissipation by applying innovative cooling architectures and will also address the integration of electrical/optical interconnects for high speed data transmission. Glass interposers with through glass vias (TGV) will be used as a carrier-in-package for RF and SiP approaches. These new generations of interposers are the base line for modularized 3D stacked architectures for fully heterogeneous systems.

Research and development focus:

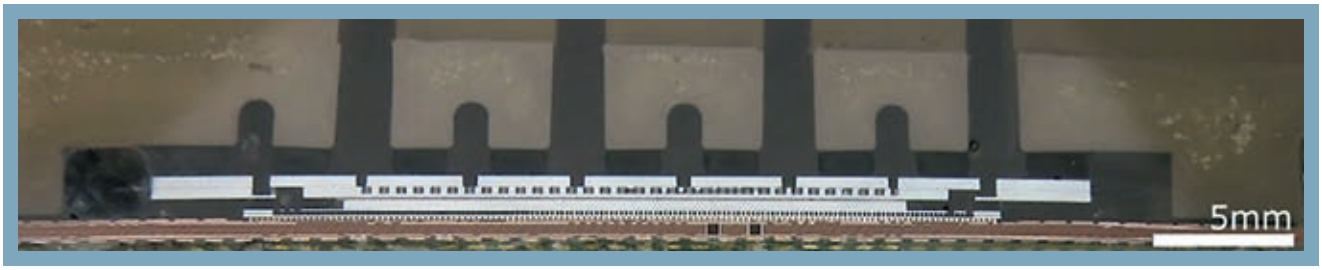
- Interposers with high-density Cu-TSV
- Glass interposers with TGV
- High-density multi-layer copper wiring: > 2 µm line/space, 4-layer frontside RDL, up to 3-layer backside RDL
- Integration of passive devices (R, L, C)
- Embedding of active and passive devices
- Interposer-based wafer-level packages
- Interposer with integrated microfluidic channels, TSV, electrical and optical interconnects and high-density routing

3D-ASSEMBLY AND INTERCONNECTION TECHNOLOGIES

Assembly and interconnection technologies relevant for 3D system integration are strongly affected by IC technology nodes. Key parameters include die size, number of I/O, pad geometries, passivation layers, wafer-surface topologies, terminal pads and limitations to the thermal budgets that can be applied during assembly. Additional challenges in assembly and interconnect technologies for 3D systems include alignment accuracy, yield requirements and productivity that meet the demands of cost effective manufacturing.

Research and development focus:

- Evaluation of die-to-wafer (D2W), die-to-interposer (D2IP) and wafer-to-wafer (W2W) assembly technologies
- 3D IC assembly with high-density interconnects (> 1000 I/O) and ultra-fine pitch (> 50 µm)
- IC assembly with thin and ultra-thin chips (20 – 150 µm)
- Evaluation of low-temperature assembly technologies
- Evaluation of flux-free solder connections with self-alignment capability



CUSTOMER SERVICES

Technological services include:

- Customer-specific prototyping (WL-SiP, TSV interposer) and pilot line manufacturing
- Material and equipment evaluation, process development, process transfer and product integration
- TSV silicon interposer
- 3D TSV via middle/via last, backside via last process integration
- Deposition and patterning of dielectric polymers, CVD dielectrics and metal films, Cu damascene processing
- Multi-layer Cu redistribution with customer-specific terminal pad metallurgies (Cu, Cu/Ni/Au, Cu/SnAg)
- Wafer thinning and thin wafer processing
- ECD WL bumping (Cu-Pillar, SnAg, CuNiAu)
- WL assembly and stacking (D2W, W2W)

Forschungsfabrik Mikroelektronik Deutschland

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2016 3DInCites AWARDS WINNER

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CONTACT

Director Fraunhofer IZM
Prof. Dr.-Ing. Martin Schneider-Ramelow
Phone: +49 30 46403 153
E-Mail: martin.schneider-ramelow@izm.fraunhofer.de

Fraunhofer IZM-ASSID
Ringstr. 12
01468 Moritzburg, Germany
Phone: +49 351 795572 0 |
www.izm.fraunhofer.de

Management IZM-ASSID
Head of Division Wafer Level System Integration
Dr. Manuela Junghähnel
Phone: +49 351 795572 0
E-Mail: manuela.junghaehnel@assid.izm.fraunhofer.de

Dept. Head of Division Wafer Level System Integration / Lithography and Polymers
Dr. Frank Windrich | +49 351 795572 49
E-Mail: frank.windrich@assid.izm.fraunhofer.de

BEoL Metallization
Catharina Rudolph | +49 351 795572 61
E-Mail: catharina.rudolph@assid.izm.fraunhofer.de

Pre-Assembly, Wafer Bonden
Dr. Andreas Gang | +49 351 795572 62
E-Mail: andreas.gang@assid.izm.fraunhofer.de

3D Process Integration
Kay Viehweger | +49 351 795572 53
E-Mail: kay.viehweger@assid.izm.fraunhofer.de

Metrology and Analysis
Dr. Wolfram Steller | +49 351 795572 86
E-Mail: wolfram.steller@assid.izm.fraunhofer.de

Micro-Nano Interconnect (Cooperation with TU Dresden / IAVT)
Jun.-Prof. Dr. Iuliana Panchenko | +49 351 795572 814
E-Mail: iuliana.panchenko@assid.izm.fraunhofer.de

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